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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,970	11/21/2003	Yoshifumi Tanada	12732-178001 / US6774	8011

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EXAMINER	
SHERMAN, STEPHEN G	
ART UNIT	**PAPER NUMBER**
2629	

DATE MAILED: 11/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,970	TANADA ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-12 and 19-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-12 and 19-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 October 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed the 10 October 2006. Claims 1-6, 8-12 and 19-23 are pending. Claims 7 and 13-18 have been cancelled.

Response to Arguments

2. Applicant's arguments with respect to claims 1-6, 8-12 and 19-23 have been considered but are moot in view of the new ground(s) of rejection. The examiner notes that the new grounds of rejection for claim 1 is based upon the change of the claim limitation that "any one of the first to n-th light-emitting elements is sequentially selected and emits light" to "each of the first to n-th light-emitting elements emits light in a field sequential driving format, and n is a natural number, $2 \leq n$." The new grounds of rejection for claims 2 and 3 is based the addition of the claim limitation that "the m-th light emitting layer is interposed between the m-th pixel electrode and the (m+1)th pixel electrode," and also in claim 2 the addition of "a pixel comprising." The new grounds of rejection for claim 19 is based upon the addition of the limitation that "the first to n-th light emitting elements as laminated, and n is a natural number, $2 \leq n$."

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1, 19-20 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokimoto et al. (EP 1 204 087 A1) in view of Sheats et al. (US 6,965,361).

Regarding claim 1, Tokimoto et al. disclose a display device comprising:

a pixel comprising first to n-th light-emitting elements that emit different emission colors (Figure 7 shows the configuration of a pixel which includes light emitting elements 11, 12 and 13 which emit red, green and blue color.),

wherein:

each of the first to n-th light-emitting elements emits light in a field sequential driving format, and n is a natural number, 2≤n (Figure 8 and paragraphs [0058]-[0059] explain that the red, green and blue LEDs are each selected sequentially in order to emit light. Paragraphs [0060]-[0063] explain that the red is selected, then the green, and then the blue and that this is repeated every period meaning that in every period, i.e. field, that each color is elected sequentially.).

Tokimoto et al. fail to teach wherein the first to n-th light emitting elements are laminated.

Sheats et al. disclose of a display having LEDs in which the LEDs are laminated (Column 3, lines 36-42 explain that the LEDs are laminated on the TFT substrate.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to make the LEDs taught by Tokimoto et al. laminated as taught by Sheats et al. in order to provide an LED display which has a cost effective manufacturing process by utilizing roll-to-roll processing techniques on polymer films and which does not require the deposition of the transparent electrode onto the already deposited layers.

Regarding claim 19, Tokimoto et al. disclose a driving method of a display device comprising the steps of:

sequentially selecting any one of first to n-th light-emitting elements that are included in pixels and emit different emission colors (Figure 8 and paragraphs [0058]-[0059] explain that the red, green and blue LEDs are selected sequentially.);

controlling potential between two electrodes of the selected light-emitting element (Paragraph [0057] explains that the two electrodes of the LEDs are connected between a current source and a power source and that a switch controls the connection to the power source Vcc in order to control the potential between the two electrodes of the LED.); and

sequentially causing the light-emitting element to emit light (Figures 7 and 8 and paragraphs [0057]-[0059] explain that the red, green and blue LEDs sequentially emit light.).

wherein:

n is a natural number, $2 \leq n$ (Figure 7 shows that there are more than 2 light emitting elements.).

Tokimoto et al. fail to teach wherein the first to n-th light emitting elements are laminated.

Sheats et al. disclose of a display having LEDs in which the LEDs are laminated (Column 3, lines 36-42 explain that the LEDs are laminated on the TFT substrate.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to make the LEDs taught by Tokimoto et al. laminated as taught by Sheats et al. in order to provide an LED display which has a cost effective manufacturing process by utilizing roll-to-roll processing techniques on polymer films and which does not require the deposition of the transparent electrode onto the already deposited layers.

Regarding claim 20, Tokimoto et al. and Sheats et al. disclose the semiconductor device according to claim 1.

Sheats et al. also disclose wherein the semiconductor device is one selected from the group consisting of an EL display, a video camera, a personal computer, a portable information terminal, a mobile telephone, and a digital camera (Column 1, lines 13-19 and 37-44 explain that LED displays can be used in portable computer, i.e. personal computer.).

Regarding claim 23, Tokimoto et al. and Sheats et al. disclose the driving method according to claim 19.

Sheats et al. also disclose wherein the semiconductor device is one selected from the group consisting of an EL display, a video camera, a personal computer, a portable information terminal, a mobile telephone, and a digital camera (Column 1, lines 13-19 and 37-44 explain that LED displays can be used in portable computer, i.e. personal computer.).

6. Claims 2-6, 8-12 and 21-22 rejected under 35 U.S.C. 103(a) as being unpatentable over Knapp et al. (US 2003/0117348) in view of Sheats et al. (US 6,965,361).

Regarding claim 3, Knapp et al. disclose a display device comprising:

a pixel comprising:

first to (n+1)th pixel electrodes;

first to n-th light-emitting layers that emit different emission colors (Figure 4 shows display elements 11a-11c which have light-emitting layers such that 11a emits red light, 11b emits blue light and 11c emits green light.);

a transistor for switching (Figure 4, transistor 16); and

first to n-th transistors for driving (Figure 4, transistors 21-22. The examiner interprets from paragraphs [0064]-[0065] and [0071] that the shunt transistors 22 work in conjunction with the driving transistor 12 to drive the display elements 11a-11c, therefore making the transistors drive transistors used for driving the display.);

a source signal line (Figure 4, data line 17);

a gate signal line (Figure 4, gate line 15);

first to n-th current supply lines (Figure 4, control lines 23 are explained to carry current in paragraph [0065].)); and

a power line (Figure 4, item 21);

wherein:

the m-th light emitting layer is interposed between the m-th pixel electrode and the (m+1)th pixel electrode (Figure 4 shows display elements 11a-11c which have pixel electrodes on either side of the light emitting elements, where the light emitting material inside of the LEDs is interposed between two pixel electrodes.),

a gate electrode of the transistor for switching is electrically connected to the gate signal line (Figure 4, the gate of transistor 16 is connected to gate line 15.),

a first electrode of the transistor for switching is electrically connected to the source signal line (Figure 4, the transistor 16 is connected to the data line 17.),

a second electrode of the transistor for switching is electrically connected to gate electrodes of the first to n-th transistors for driving (Figure 4, the transistor 16 is connected to the gate of driving transistor 12 which is in turn connected to the gates of transistors 22.),

the m-th pixel electrode is electrically connected to the m-th current supply line via the m-th transistor for driving (Figure 4 shows that display elements 11a-11c are connected to the current supply lines 23 through transistors 22.), and

the (n+1)th pixel electrode is electrically connected to the power line (Figure 4 shows that display element 11c has a last electrode connected to the power source 21.),

the potential difference between the pixel electrodes sandwiching the m-th light-emitting element is sequentially adjusted so that the m-th light emitting element selectively emits light (Figure 4 shows display elements 11a-11c which have pixel electrodes on either side of the light emitting elements, where the light emitting material inside of the LEDs is interposed between two pixel electrodes, meaning that the light emitting layer will emit light when the electrodes surrounding it are adjusted.),

n is a natural number, $2 \leq n$, and

m is a natural number, $1 \leq m \leq n$.

Knapp et al. fail to teach wherein the first to n-th light emitting layers and the first to n-th pixel electrodes are laminated.

Sheats et al. disclose of a display having LEDs in which the LEDs are laminated (Column 3, lines 36-42 explain that the LEDs are laminated on the TFT substrate.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to make the LEDs taught by Tokimoto et al. laminated as taught by Sheats et al. in order to provide an LED display which has a cost effective manufacturing process by utilizing roll-to-roll processing techniques on polymer films and which does not require the deposition of the transparent electrode onto the already deposited layers.

Regarding claim 2, this claim is rejected under the same rationale as claim 3.

Regarding claim 4, Knapp et al. and Sheats et al. disclose the display device according to claim 3.

Knapp et al. also disclose a display device further comprising:

a gate signal line for erasure (Figure 4, gate line 15 also acts as a gate line for erasure.);

wherein:

the pixel further comprises a transistor for erasure (Figure 4, transistors 24 are transistors for erasure.),

the gate electrode of the transistor for erasure is electrically connected to the signal line for erasure (Figure 4 shows that the gate of transistor 24 is connected to the gate line 15.),

the first electrode of the transistor for erasure is electrically connected to the gate electrodes of the first to n-th transistors for driving (Figure 4 shows that the transistors 24 are connected to the gates of transistors 22.), and

the second electrode of the transistor for erasure is electrically connected to any one of the first to n-th current supply lines (Figure 4 shows that transistors 24 are connected to the lines 23.).

Regarding claim 5, Knapp et al. and Sheats et al. disclose the display device according to claim 3.

Knapp et al. also disclose a display device further comprising:

a gate signal line for erasure (Figure 4, gate line 15 also acts as a gate line for erasure.); and

a retention volume line (Figure 4, item 41.);

wherein:

the pixel further comprises a transistor for erasure (Figure 4, transistors 24 are transistors for erasure.),

the gate electrode of the transistor for erasure is electrically connected to the gate signal line for erasure (Figure 4 shows that the gate electrode of transistor 42 is connected to gate line 15.),

the first electrode of the transistor for erasure is electrically connected to the gate electrodes of the first to n-th transistors for driving (Figure 4 shows that the transistors 42 are connected to the gates of transistors 22 through capacitors 43.), and

a second electrode of the transistor for erasure is electrically connected to the retention volume line (Figure 4 shows that the transistors 42 are connected to the line 41.).

Regarding claim 6, Knapp et al. and Sheats et al. disclose the display device according to claim 3.

Knapp et al. also disclose a display device further comprising:

a gate signal line for erasure (Figure 4, gate line 15 also acts as a gate line for erasure.);

wherein:

the pixel further comprises first to n-th transistors for erasure (Figure 4, transistors 42 are transistors for erasure.);

the gate electrodes of the first to n-th transistors for erasure are electrically connected to the gate signal line for erasure (Figure 4 shows that the gate electrode of transistor 42 is connected to gate line 15.), and

the first to n-th transistors for erasure are disposed between the first to n-th pixel electrodes and the first to n-th transistors for driving (Figure 4 shows that transistors 42 are disposed between driving transistor 12 and elements 11a-11c.).

Regarding claims 8-12, Knapp et al. and Sheats et al. disclose the display device according to claims 2-6.

Knapp et al. and Sheats et al. fail to explicitly teach wherein the second to n-th pixel electrodes all comprise a transparent substance, however, it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to make the pixel electrodes transparent in order to allow light to pass through the electrodes to create the display and prevent light from being blocked.

Regarding claim 21, Knapp et al. and Sheats et al. disclose the semiconductor device according to claim 2.

Sheats et al. also disclose wherein the semiconductor device is one selected from the group consisting of an EL display, a video camera, a personal computer, a portable information terminal, a mobile telephone, and a digital camera (Column 1, lines 13-19 and 37-44 explain that LED displays can be used in portable computer, i.e. personal computer.).

Regarding claim 22, Knapp et al. and Sheats et al. disclose the semiconductor device according to claim 3.

Sheats et al. also disclose wherein the semiconductor device is one selected from the group consisting of an EL display, a video camera, a personal computer, a portable information terminal, a mobile telephone, and a digital camera (Column 1, lines 13-19 and 37-44 explain that LED displays can be used in portable computer, i.e. personal computer.).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nathan et al. (US 2004/0129933) disclose of a display in which each pixel comprises a red, green and blue LED (Figure 16).

Winters (US 2004/0222746) discloses of a display in which each pixel comprises a red, green and blue LED (Figure 2).

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

6 November 2006

AMR A. AWAD
SUPERVISORY PATENT EXAMINER